A 1.2 THz Planar Tripler Using GaAs Membrane Based Chips

J. Bruston*, A. Maestrini, D. Pukala, S. Martin, B. Nakamura and I. Mehdi

Jet Propulsion Laboratory, California Institute of Technology, Pasadena, CA 91109
**now at ESA-ESTEC, Noordwijk, NL*

1 ABSTRACT

Fabrication technology for Submillimeter-wave monolithic circuits has made tremendous progress in recent years and it is now possible to fabricate sub-micron GaAs Schottky devices on a number of substrate types, such as membranes [1], frame-less membranes [2] or substrateless circuits [3]. These new technologies allow designers to implement very high frequency circuits, either Schottky mixers or multipliers, in a radically new manner.

This paper will address the design, fabrication, and preliminary results of a 1.2 THz planar tripler fabricated on a GaAs frame-less membrane, the concept of which was described previously [2]. The tripler uses a diode pair in an antiparallel configuration similar to designs used at lower frequency [4]. To date, this tripler has produced a peak output power of 80 μW with 0.9% efficiency at room temperature (at 1126 GHz). The measured fix-tuned 3 dB bandwidth is about 3.5%. When cooled, the output power reached a peak of 195 μW at 120 K and 250 μW at 50K. The ease with which this circuit was implemented along with the superb achieved performance indicates that properly designed planar devices such as this tripler can now usher in a new era of practical very high frequency multipliers.

2 INTRODUCTION

For a number of years astrophysicists and radio astronomers have been demanding a full submillimeter survey-type mission to investigate phenomena such as star formation and galaxy evolution. The Far Infrared and Submillimeter Telescope, FIRST [5], now renamed the Herschel Space Observatory, HSO, is the most comprehensive mission for these frequencies. In the initial planning of HSO it became obvious that while the detector elements have improved considerably over time the available technology for broad band local oscillator sources left much to be desired. Cascaded multipliers following a fundamental driving source have been the working horse of local oscillators for years For mass and volume reasons, solid state technology is favored over heavy and bulky molecular lasers, although these are being used when the mission permits [6. Unfortunately limitations on maximum output power didn't allow their use for flight above about 300 GHz (although lab demonstrations had been done up to 1.4 THz [7].) First made with whisker contacted diodes, frequency multipliers have recently been developed with the preferred, more reliable, more reproducible, and easier to assemble, planar technology. Improvements in GaAs processing technology have allowed for the design of GaAs Schottky varactor multipliers up to the higher end of the submillimeter-wave range.

In our attempt to push the fully integrated Schottky diode technology to supra THz frequencies, we have benefited from the recently available power amplifiers that operate around 100 GHz [8],

along with improvements in multipliers at sub-terahertz frequency [3]. Previously, we introduced the frameless membrane and presented a number of design concepts to reach supra THz frequency [2]. This paper will detail the concept and final design methodology, fabrication and preliminary test of a GaAs membrane based 1.2 THz tripler. We believe that the work presented in this paper is a major step in meeting this challenge of implementing supra-THz Local Oscillator for space-borne receivers.

3 DESIGN AND FABRICATION

GaAs membrane based planar Schottky devices have been demonstrated as mixers at 2.5 THz, with very impressive results [1, 6]. They use a 3 μm thick GaAs membrane suspended across the RF waveguide by means of a sturdier, 50 μm thick GaAs frame. This requires that the waveguide be perpendicular to the membrane, as a traditional split waveguide block would see the thick, high dielectric constant, lossy frame in the waveguide. This results in several design constraints. To gain in design flexibility, we decided to design and fabricate devices without any frames [2]. Handling and assembly turned out not to be an issue, as we will discuss later. To allow for "drop-in" assembly, and provide simple bias connections, we decided to make extensive use of beam leads. The availability of the membrane allows one to move the diodes away from the waveguides, to which they are coupled by means of stripline matching circuits and waveguide probes. The main advantage of using diodes remote from the waveguides is that it simplifies the diode analysis and optimization. Also, and in the case of a balanced tripler, the quasi TEM coplanar structure with grounds on chip permits the two diodes to be biased in series, simplifying the biasing circuit. Finally, it ensures that only the TEM mode propagates at every harmonic, simplifying the matching circuit design. The ground planes are shorted to the block by means of wide beam leads, which also provide support for the membrane assembly [2]. A sketch of the final design is shown in Figure 1.

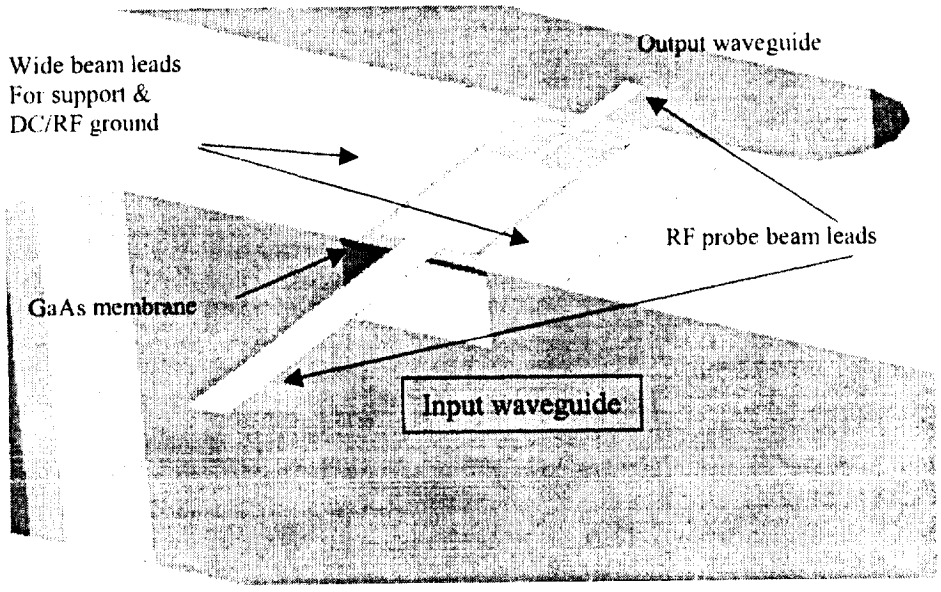

Figure 1: *Final design of the frameless tripler is shown placed inside the split waveguide block.*

3.1 Device optimization and Diode loop

The tripler utilizes a diode pair in an antiparallel configuration similar to designs used at lower frequency [4]. This configuration has the distinct advantage that only odd harmonics are generated. However, it requires a carefully designed second harmonic idler tuning circuit. The second harmonic current flows in the diode loop (fig. 2a), which needs the adequate series reactance for resonating the third harmonic [9]. The value of this reactance can be calculated, like the other embedding impedance of the diode, by means of harmonic balance simulation and optimization. We used our in house diode model of the JPL made planar Schottky diode [10], that we updated for THz frequency, introducing harmonic dependent series resistance. The optimum diode doping and size is found using only one diode and half the input power. We used a doping of $5x10^{17}$ cm^{-3} and an anode of $0.4x1.3$ μm^2. However, this approach can not provide the embedding impedance of the final configuration. The reactive series impedance required for the idler in the diode loop directly impact the embedding impedance at the first and third harmonic. It is therefore important to first optimize this loop and then calculate the embedding impedance.

Our approach was semi empirical and iterative. The diodes, the diode mesas, and the air bridges constitute the diode loop (fig. 2 b and c). A first step consisted of developing an electrical equivalent circuit for this structure, where the air bridges are replaced by inductances modeled as suspended ribbon (fig. 2 a). This allows a first optimization leading to a starting value of the inductance for best idler tuning. In turn, this inductance permits the definition of the corresponding air bridges (the mesas dimensions were fixed in the design, by fabrication considerations). However, this approach is approximate, and the inductance value in the diode loop is not well described by the equivalent model. This is due to the fact that the idler reactance is also impacted by the dimensions of the channel in which the circuit resides. We therefore use the now well developed technique of 3D electromagnetic simulation [10] (with Ansoft HFSS) to evaluate the inductance in the loop (fig. 2 b). The computed S-parameters of the structure are inserted into the harmonic balance for performance calculation. This time, we use terminations only at the first and third harmonics, as the second harmonic idler is contained in the S-parameters. Fine tuning of the air bridges length and width permits some further performance improvement. However, we never matched the diode maximum performance computed with ideal embedding impedance and idler. The air bridge length and width provide some flexibility in tuning the inductance, but one must also tune the cavity in which the circuit resides to obtain optimum values. However, for our first iteration, we decided not to use this parameter as a tuning variable, to simplify the design. This shall be optimized in future iterations. In spite of this, the compromised performance is a good trade off. As a matter of fact, the idler inductance makes the diode structure very high Q at the third harmonic, compromising the final design bandwidth. The non-optimum idler reduces this effect, allowing for a relatively wide band design.

3.2 Waveguide probes

Removing the diodes from the waveguide, either input or output, provides a safe quasi TEM mode environment for the diodes and circuits, together with a simple bias scheme. Furthermore, it allows us to separate carefully the different issues inherent to this kind of design: the diode optimization and implementation, the waveguide to planar circuit transitions, the waveguide to open propagation (horn, see below), and finally the matching between the different pieces.

One doesn't need to design the CPW to waveguide probe to have any particular impedance termination, as the matching circuit between the probes and the diodes does not need to transform to 50 Ohms, the value usually used to design probes. The impedance of the diodes nominally has a fairly low real part and some reactive part. It will greatly help the matching circuit design to obtain a probe termination impedance close to the diode's conjugate impedance.

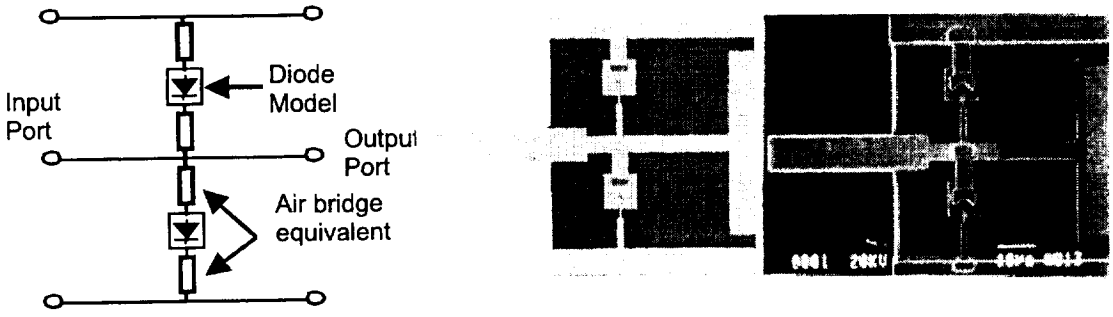

***Figure 2**: (a) The diodes have an antiparallel configuration restraining the second harmonic current in the diode loop. This loop must have the right impedance at the second harmonic to maximize third harmonic production. (b) The diode structure as simulated with HFSS showing the mesas and air bridges part of the diode loop seen by the second harmonic current. (c) Photograph of the same diodes after fabrication.*

We used this philosophy in our design, picking any probe dimension (length and width) that we knew would work somewhat without introducing too much resonance. We only provided for length optimization, by simulating a few with HFSS and, having inserted the aggregate results as a 2 dimensional matrix in the harmonic balance, letting the simulator extrapolate the best length. This worked so well that we actually found an output probe with a termination impedance almost perfectly matching the diodes at the third harmonic. This is a great result, as this means the diodes could be almost in the plane of the transition, which, due to the waveguide cut-off, provides for the required first harmonic short without the need for additional lossy circuit features. However, this also introduced an iteration in the calculation of the embedding impedance, as the close proximity of the diodes to the output waveguide, meant that some effect due to evanescent modes had to be taken into account.

The probes are designed as metal beam leads, with all the GaAs removed from the waveguide. This implementation yields a wider bandwidth transition and reduced loss. The aspect ratio of the probe (20 μm wide, 175 μm long, 1 μm thick) provides enough mechanical robustness and sturdiness.

3.3 Matching circuit

The output match was non existent as the probe provided the right impedance. The remaining match, to the horn, was made using waveguide sections (see below).

The input matching circuit had to match from the diode impedance at the first harmonic to the input waveguide probe impedance, together with providing a short at the third harmonic. This

was done using a two sections high-low impedance Chebyschev transformer. It is desirable to work with a small number of sections, in order to reduce loss, and maintain a small robust circuit. The price is reduced bandwidth. As we did not need to go through 50 Ohms, two sections provided sufficient bandwidth and a simpler design for our first iteration. If the bandwidth appears too narrow, additional sections can be added in subsequent design iterations.

3.4 Bias circuit

The diode optimization and performance computation showed an optimum bias close to 0V. This allowed for an unbiased nominal circuit design, which would provide testable devices in the event that implementation of the bias circuit failed. However, we provided for bias on some circuits, to help debugging, and to test the concept for future designs that may require bias.

Since the two diodes are in series between the two ground planes of the CPW circuit, to provide for bias, we needed to keep one ground plane, via its beam lead, DC grounded, by shorting to the block. The connection of the diodes to the opposite ground plane, therefore, has to provide for DC decoupling. The solution is to run an air bridged interconnect line from one of the diodes to a MIM capacitor on the CPW ground plane. This capacitor provides for RF short and DC decoupling. A narrow, high inductance MIM line connects the capacitor to a DC bond pad located in a side channel in the block. The quasi TEM mode nature of the circuit prevents any leakage of the RF through the bias channel. We ensured that was the case using HFSS simulation of the whole structure and looking at RF leakage at the end of the channel.

However, the narrow ground plane on membrane didn't provide much space for the MIM decoupling capacitor. The calculated capacitor impedance at the first harmonic is 4 Ohms. In spite of this fairly high value, the measured results show that the bias circuit has little, if any, impact on performance. Figure 3 shows the bias circuit after fabrication.

3.5 Housing block and output horn

The housing block uses a traditional split waveguide configuration, with the tripler chip positioned in a channel joining the two parallel waveguides. This configuration allows for in line input - output waveguides, low loss waveguide split as the cut is placed in the E plane of the TE_{10} dominant mode, and simple machining using high precision NC milling tools.

The 400 GHz input waveguide is terminated by an in house designed flange used as a standard for all our high frequency designs. The transition from the output waveguide to free space propagation is made by means of a built-in transition from rectangular to circular waveguide and Picket Potter horn [11].

3.6 Circuit fabrication

The membrane chip fabrication was described in detail in [2]. Extensive use of a projection aligner, dry etch techniques and etch stop layers all contributed to high circuit yields. The biasable circuits had somewhat reduced yields, due to the presence of circuit designs with thick GaAs support frames that interfered with some of the backside lithography. This problem could be eliminated in the future by processing the 1.2 THz circuits separately. The fabricated chip is shown in fig.3.

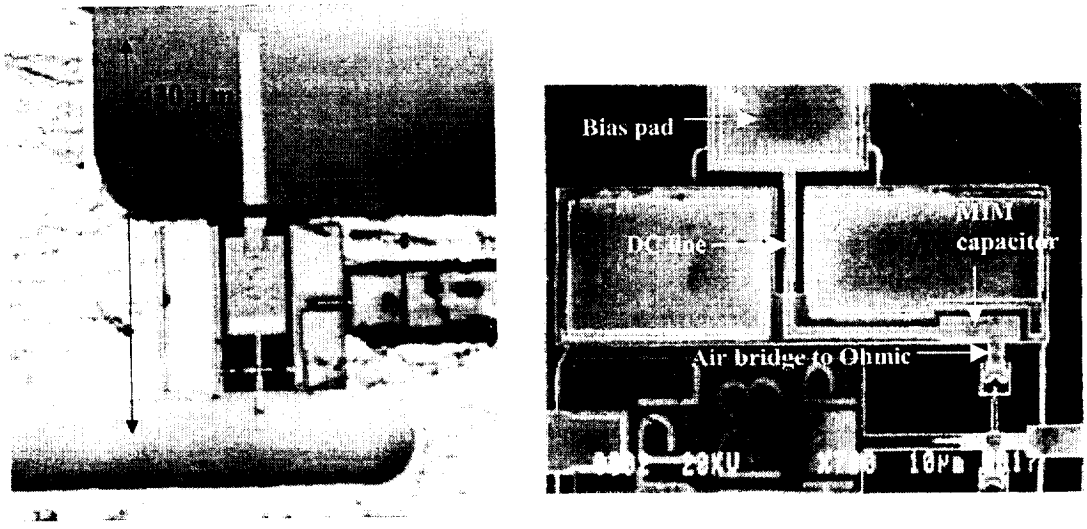

Figure 3: a) A fabricated 1.2 THz tripler after assembly into the waveguide block, showing bias circuit, RF probes and "drop in" support beam leads. b) SEM of the bias circuit showing MIM capacitor with Air-bridge to ohmic, and DC line to bias pad.

4 PERFORMANCE

4.1 Simulation

It is difficult to accurately predict multiplier performance at supra THz frequencies. Performance calculation is based on harmonic balance simulation of the active elements (the Schottky diodes), and 3D electromagnetic simulation of the circuit topology (mesas and air bridges, CPW matching circuit, waveguide to CPW transitions, etc.).

The harmonic balance accuracy relies on the analytical model developed for the JPL made Schottky diode [10]. This model has been verified at least to 100 GHz by means of comparison to vector network measurements of JPL diodes. However, several effects render this model approximate at supra THz frequencies [12]. When the classical model is used (as described in [10]), we find a tripling efficiency of about 8%. This is obviously an overestimation. An improved model, including a frequency dependent series resistance (Rs) that more than triples its value at the third harmonic (1.2 THz) yields an efficiency of about 2 %. To further evaluate the impact of Rs on performance, we can apply a correction factor, as illustrated in figure 4b. As will be seen later, measurements yielding efficiencies of nearly 1% indicate that a correction factor of no more than 1.5 is necessary at these frequencies. In any case, current models provide a 3 dB estimation of the performance, which while not perfect can allow for further optimization of the device structure.

Similarly, the accuracy of the 3D electromagnetic simulation relies on the ability to simulate the fabricated structure. At supra THz frequencies, small details such as mesa height, ignored at sub THz frequencies, become important parameters. However, simulating these fine structures becomes computationally intensive, and often it is not possible to obtain convergence. Furthermore, the sheer size of these features is within the accuracy of device fabrication, and it becomes difficult to guaranty exact feature sizes.

These restrictions make the prediction of performance somewhat academic at supra THz frequencies. However, as part of the design process, this calculation is used to establish a nominal design. Doing so, we found a calculated performance of better than 1% over a 15% bandwidth centered around 1200 GHz, with 10 mW input power. The design performance is summarized in Fig 4a.

Finally, it is important to evaluate the tolerance of our design to one of the most critical fabrication issue, the anode size. Using the tools described above, we were able to calculate the efficiency of the tripler as a function of the anode length. This simulation shows a clear optimum, close to the designed length value. One important result is that, although the performance degradation can reach 50% for a 50% change in anode size, it is negligible for variations within 20% of nominal. As illustrated by figure 4, the efficiency is more strongly influenced by small variations on the series resistance model than by anode size for a fixed model.

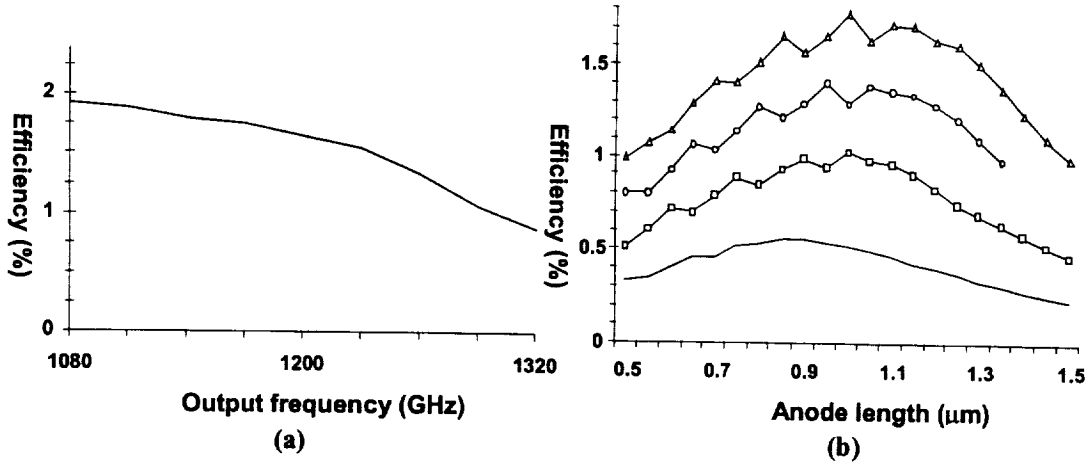

Figure 4: *a) Efficiency as a function of frequency, for the final tripler design computed with harmonic balance, using JPL diode model, and S-parameters from Ansoft HFSS: input power is 10 mW over 360 to 440 GHz, 0V bias.* ***b)*** *Efficiency as a function of anode length and series resistance, with 10 mW input power at a fixed frequency of 400 GHz, and 0V bias. It is important to note that these results are for the specific design, and not the intrinsic diode performance with ideal embedding.*

4.2 Assembly

Assembly of the tripler chip in the housing block is made straight forward by the "drop-in" approach. As the nominal device needs no bias, it is sufficient to drop the chip in place, tuning its

position for proper probe alignment in the waveguides. The mating of the two halves of the split housing waveguide block holds the chip in place by "clamping" the ground beam leads thus ensuring a good RF ground. No soldering or bonding is necessary. The assembly of the biasable version requires a more complex procedure, as it is necessary to either bond or solder the DC feed to the bias pad that extends from the membrane. The original design did not permit bonding, and soldering is difficult due to the small size of the pad. A new design shall provide for clamping the bias pad beam lead in a similar manner to the ground beam leads.

4.3 Measurements

Preliminary measurements have been performed using the set up described in [13]. The tripler is driven using a 400 GHz solid state source composed of a 100 GHz HEMT power amplifier module [8] followed by two doublers. The fundamental source is a 100 GHz BWO used for convenience and lab availability. This chain delivers a peak output power of approximately 8mW at 375 GHz. The 1.2 THz tripler output power is measured by means of a Thomas Keating calorimeter [13].

Room temperature RF measurements of the tripler have provided a maximum output power of about 70 μW at 1126 GHz, or a 0.9% conversion efficiency, with a 3 dB fix-tuned bandwidth of 3.5 %. Measured output power of the tripler along with the input power are shown in Figure 5. Note that there are no movable tuners on the entire chain. The output power follows the input power level and the efficiency is fairly independent of frequency over the measured band. This performance is achieved with the smaller than nominal anode of 0.9x0.4 μm2, as the nominal design (1.3 x 0.4 μm2) was optimized for 10 mW of input power. With only 8 mW of input power, the nominal diodes are under-pumped, hence the need for a smaller anode to provide a diode impedance compatible with the circuit. This is encouraging, as we think that the design will show an increased efficiency and bandwidth with an increased and flat input power profile.

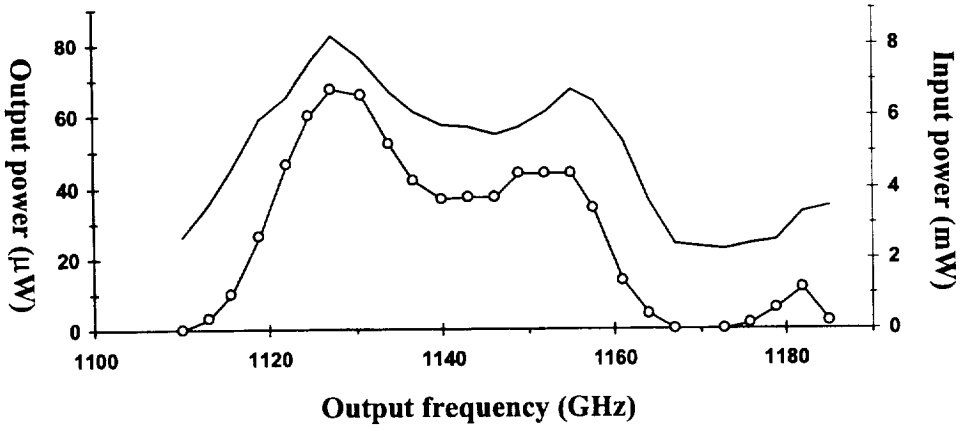

***Figure 5**: Measured frequency response of the fix-tuned tripler along with the available input power. The bandwidth and maximum output are restricted by the limited input power.*

Room temperature measurements made with a different first stage doubler yielding higher power at 400 GHz provided 80 μW, or 0.9 % efficiency, at 1126 GHz. When cooled, the two doublers and tripler chain yielded 195 μW at 120K, and 250 μW at 50K.

Measurements of the biased chip were made with the nominal size anode devices only, as the other anode sizes lacked bias circuitry. The biased chips did not show any improved performance when compared to non biased ones of similar size. Furthermore, the optimum bias voltage was found to be close to 0 V, confirming our design analysis.

5 CONCLUSION

We have designed, fabricated and done preliminary measurements on a 1.2 THz planar tripler that incorporates a free standing GaAs membrane and multiple beam leads. This design has proven robust, easy to assemble, with, at the time of this writing, record performance for a supra THz multiplier. This result validates the use of integrated planar technology for THz multiplier, and demonstrates the viability of the technology for projects such as HSO.

6 ACKNOWLEDGEMENTS

We are highly appreciative of the numerous technical discussions that we have had with Neal Erickson (UMass), Peter Zimmermann (RPG), Chris Mann (RAL) and Tom Crowe (UVa). We also wish to acknowledge the technical help provided by Pete Bruneau and Ray Tsang (of JPL) for block fabrication and device assembly respectively. The research described in this publication was carried out at the Jet Propulsion Laboratory, California Institute of Technology, under a contract with the National Aeronautics and Space Administration

7 REFERENCES

[1] P.H. Siegel, R.P. Smith, S. Martin and M. Gaidis, "2.5 THz GaAs Monolithic Membrane-Diode Mixer",*I EEE Transactions Microwave Theory and Techniques*, vol. 47, no. 5, pp. 596-604, May 1999.

[2] J. Bruston, S. Martin, A. Maestrini, E. Schlecht, R.P. Smith, I. Mehdi, "The Frame-less Membrane: A Novel Technology for THz Circuits," *Proc. Eleventh International Symposium on Space THz Technology*, Ann Arbor, May 2000.

[3] E Schlecht, J. Bruston, A. Maestrini, S. Martin, D. Pukala, R. Tsang, A. Fung, R. P. Smith , I. Mehdi, "200 And 400 GHz Schottky Diode Multipliers Fabricated with Integrated Air-Dielectric "Substrateless" circuitry," *Proc. Eleventh International Symposium on Space THz Technology*, Ann Arbor, May 2000.

[4] C.P. Hu, "Millimeter wave frequency multipliers employing semiconductor diodes in a balanced configuration," *Proc. 16th European Microwave Conf.*, Dublin 1986, 247-251.

[5] G. Pilbratt, "The FIRST mission," *Proc. ESA Symp., The Far Infrared and Submillimetre Universe 1997*, ESA SP-401

[6] Michael C. Gaidis, Herbert M. Pickett, C. D. Smith, Suzanne C. Martin, R. Peter Smith, and Peter H. Siegel, "A 2.5 THz Receiver Front End for Spaceborne Applications," *IEEE Trans. Microwave Theory and Tech.*, v. 48, no. 4, April 2000, pp. 733-739.

[7] P. Zimmermann, *private communication.*

[8] L. Samoska, T. Gaier, A. Peralta, S. Weinreb, J. Bruston, I. Mehdi, Y.C. Chen, H.H. Liao, M. Nishimoto, R. Lai, H. Wang, Y.C. Leong, "MMIC Power Amplifiers as Local Oscillators for FIRST," *Proc. SPIE UV, Optical, and IR Space Telescopes and Instruments*, SPIE 4013, Munich, Germany, March 2000, not yet published

[9] P. Penfield, R.P. Rafuse, "Varactor Applications," M.I.T Press, 1962.

[10] J. Bruston, R.P. Smith, S.C. Martin, A. Pease and P.H. Siegel, "Progress Toward the Realization of MMIC Technology at Submillimeter Wavelengths: A Frequency Multiplier to 320 GHz," *Proc. IEEE Intl. Microwave Symp. Dig.*, Baltimore, MD, June 1998, pp. 399-402.

[11] H.M. Pickett, J.C. hardy and J. Farhoomand, "Characterization of a Dual Mode Horn for Submillimeter Wavelengths," *IEEE Trans. Microwave Theory and Techniques,* vol. MTT-32, no. 8, pp. 936-8, Aug. 1984.

[12] J. Grajal, V. Krozer, E. Gonzalez, F. Maldonado, and J. Gismero, "Modeling and Design Aspects of Millimeter-Wave and Submillimeter-wave Schottky Diode Varactor Frequency Multipliers," *IEEE Transactions Microwave Theory and Techniques*, vol. 48, no. 4, pp. 700-712, April 2000.

[13] A. Maestrini, D. Pukala, F. Maiwald, E. Schlecht, G. Chattopadhyay, and I. Mehdi, "Cryogenic operation of GaAs based multiplier chains to 400 GHz", *proceeding of the 8th International Conference on Terahertz Electronics, Darmstadt*